Andes and MachineWare Collaborate on Early RISC-V Software Development for *AndesCore*™ AX45MPV

Aachen, Germany and Hsinchu, Taiwan, February 27th 2024
MachineWare GmbH and Andes Technology (TWSE:6533), a leading supplier of high-efficiency, low-power 32/64-bit RISC-V processor cores and Founding Premier member of RISC-V International announce an exciting new chapter in their collaboration, marked by a strategic partnership. This synergistic alliance is geared towards the highly innovative *AndesCore*™ **AX45MPV**, a cutting-edge multi-core RISC-V vector processor tailored for AI workload acceleration and the application level. In this joint effort, MachineWare lends its support by seamlessly integrating the **AX45MPV** into their **SIM-V** high-performance simulation solution. This integration proves invaluable for software developers, enabling them to efficiently handle intricate AI and Linux stack related workloads. The result is a platform that streamlines development, testing, and software verification well in advance of physical prototypes emerging from the fabrication process. This partnership underscores the mutual commitment of MachineWare and Andes Technology to advancing processor technology.

Introducing **SIM-V**, an offering from MachineWare that holds immense value for developers in the RISC-V landscape. With SIM-V, developers gain the power to thoroughly test and verify their RISC-V-based systems and software applications long before first prototypes are back from the fab. At its core, SIM-V provides a fast Instruction Set Simulator (ISS) that supports all RISC-V standard extensions. One of **SIM-V**'s notable strengths is its user-friendly customizability. Through a straightforward extension SDK, developers can swiftly integrate custom instructions, registers, and other elements into the simulator to get instant feedback on their design choices. What makes SIM-V truly special is its SystemC TLM-2.0 integration. This unique combination empowers users to seamlessly introduce their IP models into full system simulation environments, enhancing the versatility of the platform.

The AndesCore™ AX45MPV is a 64-bit 8-stage dual-issue multicore RISC-V vector processor. It incorporates RISC-V GCBP* (*P is a draft version) extensions, and supports SMP Linux with MMU (Memory Management Unit) and up to 48-bit virtual addresses. In addition, it can be configured to up to eight cores with a cache coherence manager and up to 8MB shared L2 cache memory in a cluster. The Vector Processing Unit (VPU) of the AX45MPV implements RISC-V Vector Extension (RVV) version 1.0. It supports configurations of up to 1024-bit vector width (VLEN) and datapath width (DLEN). The AX45MPV is excellent for computations involving large arrays of data such as computer vision, digital signal processing, image processing, machine/deep learning, and scientific computing.

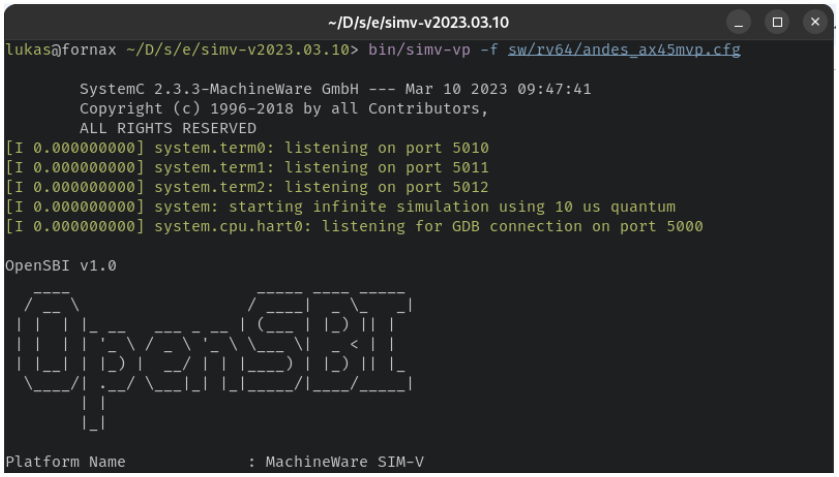

Figure 1: Invoking SIM-V with the AX45MPV configuration.

"We are delighted to join forces with Andes to support the AX45MPV processor in SIM-V," said **Lukas Jünger, Managing Director at MachineWare**. “The incorporation of the AX45MPV model enables our common customers to develop RISC-V Linux and AI software stacks and verify their functionality in minutes. This will eliminate bugs and elevate software quality all the while making the overall development process more efficient.”

"Andes’ collaboration with MachineWare is consistent with our continuous effort to broaden RISC-V ecosystem for easy adoption of high-performance simulation tools," said **Samuel Chiang, deputy marketing director of Andes Technology.** "We are excited to come together with MachineWare to drive the expansion of the RISC-V ecosystem. And we believe RISC-V's instruction set architecture will increase innovation and has the potential to transform the AI market."

About MachineWare GmbH

Founded in 2022 in Aachen, Germany, MachineWare leverages decades of experience in system level simulation and high-performance simulation tooling. Visit https://www.machineware.de/ for more details.

About Andes Technology

Nineteen years in business and a Founding Premier member of RISC-V International, Andes is a publicly-listed company (TWSE: 6533; SIN: US03420C2089; ISIN: US03420C1099) and a leading supplier of high-performance/low-power 32/64-bit embedded processor IP solutions. Its V5 RISC-V CPU families range from tiny 32-bit cores to advanced 64-bit Out-of-Order processors with DSP, FPU, Vector, Linux, superscalar, automotive and/or multi/many-core capabilities. By the end of 2023, the cumulative volume of Andes-Embedded™ SoCs has surpassed 14 billion. For more information, please visit https://www.andestech.com . Follow Andes on LinkedIn, Twitter, Bilibili and YouTube!

About ANDES RISC-V CON

ANDES RISC- V CON is the annual RISC-V technology forum of Andes Technology. In 2024, the Hsinchu session will be held at Amazing Hall Yufeng on March 28; the Shanghai session will be held at DoubleTree by Hilton Hotel Shanghai - Pudong on April 9; the Shenzhen session will be held at Grand Mercure Shenzhen Oriental Ginza Hotel on April 11. The theme of this year is "**ANDES RISC-V CON: Deep Dive into Automotive/ AI/ Application Processors and Security Trends.**" It will introduce the flexible RISC-V that revolutionizes emerging applications and share Andes latest breakthroughs and innovations in RISC-V. Four popular applications will be focused on: AI, automotive electronics, security and RISC-V's new field, application processor. Many RISC-V ecosystem partners, including TSMC, are invited to deliver talks and on-site demonstrations.
For more event details and free registration, please visit the official website of the events:

- Hsinchu: https://www.andestech.com/Andes_RISC-V_CON_2024_TW/
- Shanghai and Shenzhen: https://www.andestech.com/Andes_RISC-V_CON_2024_CN/

About RISC-V

The RISC-V open architecture ISA is under the governance of RISC-V International. Visit https://riscv.org for more details.

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